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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,976	10/06/2003	Edgardo Rulloda Hortzleza	TI-36288 (032350.B527)	6490

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EXAMINER	
DESAI, HEMANT	

ART UNIT	PAPER NUMBER
3721	

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

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Office Action Summary	**Application No.** 10/680,976	**Applicant(s)** HORTZLEZA ET AL.	
	Examiner Hemant M. Desai	**Art Unit** 3721	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

7/5/05

1. The declaration is objected to because It does not identify the city and either state or foreign country of residence of inventor named Rodel Belarmino Arquisal (Inventor No. 2). The residence information may be provided on either on an application data sheet or supplemental oath or declaration.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 6-11, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada (6119865) and Misaka (6467626) and further in view of Wu et al. (6817161).

Kawada discloses a method for shipping semiconductor wafers each having metallization subject to damage (2, fig. 1) comprising, providing a coin stacks (see fig. 2), each coin stack comprising a plurality of semiconductor wafers (1, figs. 2-3) separated from adjacent wafers by a ring-shaped wafer separator (8, figs. 2-3) and disposed within a coin stack carrier, each semiconductor wafer having a plurality of interconnection conductor material portions (2, 4, fig. 1), each coin stack further comprising first and second protection barriers (7, fig. 2) formed from foam (see col. 2, lines 37-40) and each of the wafers in the coin stack carrier has vertical orientation. Since the applicant has not defined the vertical orientation of wafers with respect to which axis, the vertical term is very broad and Kawada discloses that the position of wafers is vertical if you look at the fig. 2 by turning the figure 90°.

If to an extent that the applicant does not agree that Kawada discloses that the wafers in the coin stack has a vertical orientation. Misaka teaches by providing vertical orientation (E, F, figs. 1-2) of semiconductor wafers in a coin stack, particle adhesion to the wafers during transport can be prevented and particle inspection and cleaning of wafers transported to the wafer manufacturing process can be made unnecessary (see col. 8, lines 54-57). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to having provided the stack of semiconductor wafers having vertical orientation as taught by Misaka in the method of shipping semiconductor wafers of Kawada to prevent particle adhesion to the wafers during transport and thus particle inspection and cleaning of wafers transported to the wafer manufacturing process can be made unnecessary.

The method for shipping semiconductor wafers of Kawada as modified by Misaka meets all the claimed limitations except for positioning the coin stack carrier in a shipping box. However, Wu et al. teaches to position the coin stack carrier (20, fig. 1) in a shipping box (30, fig. 1) to prevent destruction of the coin stack carrier may occur by rough handling during transportation or by an outside influence causing shock, but more importantly, to prevent breakage of the fragile item contained within (see col. 3, lines 18-24). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to position the coin stacker carrier of Kawada in a shipping box as taught by Wu et al. to prevent destruction of the coin stack carrier may occur by rough handling during transportation or by an outside influence causing shock, but more importantly, to prevent breakage of the fragile item contained within.

The modified method for shipping semiconductor wafer of Kawada meets all the claimed limitations, except for supplying plurality of coin stacks. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide plurality of coin stacks to transport large numbers of semiconductor wafers, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

The modified method for shipping semiconductor wafer of Kawada meets all the claimed limitations, except for the vertical arrow disposed on the shipping box. However, it is well known in the art that when the content is fragile or to maintain the integrity of the contents of the shipping boxes, the arrow showing the direction to maintain the orientation in the particular direction (vertical or horizontal) and instructions to handle the shipping box in particular fashion. Applicant did not seasonally challenge the Official Notice of use of vertical arrow, and therefore the limitation in the claim is now Admitted Prior Art.

Regarding claims 4, 11 and 14, the plurality of interconnection conductor material portions (2, 4) comprises a bond pad (3, fig. 1).

Regarding claim 7, the plurality of wafer separators (8) is ring-shaped.

Regarding claim 8, the first and second protection barriers are formed from foam (see col. 2, lines 38-40).

Regarding claim 9, Kawada discloses the claimed invention except for the coin stacker carrier is formed from plastic. However, use of plastic container is well known in the packaging of semiconductor art for because it is light in weight, easy to form, and its durability and shock resistant property to prevent fragile content from breakage. Therefore, It would have been obvious to one having ordinary skill in the art at the time invention was made to form the coin stacker carrier from plastic, to prevent the semiconductor wafers from breakage, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability fro the intended use as a matter of obvious design choice. *In re Lashing*, 125 USPQ 416.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada, Misaka and Wu et al. as applied to claims 6 and 11 above, and further in view of Ambrogio (4886162).

The method for shipping semiconductor wafers of Kawada as modified by Misaka and Wu et al. meets all the limitations except for the first and second recesses in the wafer separator. However, Ambrogio teaches a wafer separator (2, fig. 1) having first recess (8, fig. 3) corresponding to an outer perimeter shape of wafer (9, fig. 3) having a first depth (see figs. 1-3) and a second recess portion formed in the wafer separator (see figs. 1-3) within the first recessed portion having a second depth so that the wafer will be properly located and the possibilities of contaminating it will be reduced to a minimum, since the peripheral wafer portion contacting the inner surface of the separator are not used for making the integrated circuits (see col. 2, lines 20-28). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to having provided the first and second recesses in the wafer separator of Kawada as taught by Ambrogio so that the wafer will be properly located and the possibilities of contaminating it will be reduced to a minimum, since the peripheral wafer portion contacting the inner surface of the separator are not used for making the integrated circuits.

5. Claims 2-3, 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada, Misaka and Wu et al. as applied to claims 1 and 6 above, and further in view of Venkateshwaran et al. (6339254).

The method for shipping semiconductor wafers of Kawada as modified by Misaka and Wu et al. meets all the limitations except for interconnection conductor material comprises a plurality of solder bumps and flip chip bumps. However, Venkateshwaran et al. teach solder bumps (611, fig. 6A) and flip chip bumps (411, fig. 6A) to reduce thermally induced mechanical stress (see col. 2, lines 64-67) and to provide stacked flip-chip assembly which is capable of having fewer external input/output connections than would be required for each of the individual chips (see col. 3, lines 11-14). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to having provided the interconnection conductor material comprises a plurality of solder bumps and flip chip bumps as taught by Venkateshwaran et al. in the semiconductor wafers of Kawada to reduce thermally induced mechanical stress and to provide stacked flip-chip assembly which is capable of having fewer external input/output connections than would be required for each of the individual chips.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawada, Misaka, Wu et al. and Venkateshwaran et al. as applied to claims 1 and 2 above, and further in view of Ambrogio (4886162).

The method for shipping semiconductor wafers of Kawada as modified by Misaka, Wu et al. and Venkateshwaran et al. meets all the limitations except for the first and second recesses in the wafer separator. However, Ambrogio teaches a wafer separator (2, fig. 1) having first recess (8, fig. 3) corresponding to an outer perimeter shape of wafer (9, fig. 3) having a first depth (see figs. 1-3) and a second recess portion formed in the wafer separator (see figs. 1-3) within the first recessed portion having a second depth so that the wafer will be properly located and the possibilities of contaminating it will be reduced to a minimum, since the peripheral wafer portion contacting the inner surface of the separator are not used for making the integrated circuits (see col. 2, lines 20-28). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to having provided the first and second recesses in the wafer separator of Kawada as taught by Ambrogio so that the wafer will be properly located and the possibilities of contaminating it will be reduced to a minimum, since the peripheral wafer portion contacting the inner surface of the separator are not used for making the integrated circuits.

Response to Arguments

7. Applicant's arguments filed 5/9/2005 have been fully considered but they are not persuasive. In response to applicant's argument that because the cited references do not recognize the source of the problem solved by the invention and there is no basis in the art for combining references. Examiner has established reasonable obviousness as set forth in the above rejection. Kawada ('865) discloses the coin stack carrier. It is well known in the art of wafer processing to transfer in vertical orientation as taught by Misaka ('626). Wu et al. ('161) teach to position the coin stack carrier in a shipping box to prevent destruction of the coin stack carrier may occur by rough handling during transportation or by an outside influence causing shock, but more importantly, to prevent breakage of the fragile item contained within. It is Admitted Prior art that when the content is fragile or to maintain the integrity of the contents of the shipping boxes, the arrow showing the direction to maintain the orientation in the particular direction (vertical or horizontal) and instructions to handle the shipping box in particular fashion. Therefore, it is obvious to a person of ordinary skill in the art to combine the references and ship the coin stack carrier in the vertical direction in the shipping box having the vertical arrow to indicate the orientation of the shipping box should be maintain to maintain the wafers in a vertical direction to maintain the integrity of the wafers in the coin stack carrier. In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. *In re Nomiya*,

184 USPQ 601 (CCPA 1915). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining reference is what the combination of disclosures take as a whole would suggest to one of the ordinary skill in the art. *In re McLaughlin*, 110 USPQ 209 (CCVA 1971). And therefore, the combination of the disclosures take as whole, as mentioned above, would suggest to one of the ordinary skill in the art to ship the coin stack carrier in the vertical direction in the shipping box having the vertical arrow to indicate the orientation of the shipping box. References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. *In re Bozek*, 163 USPQ 545 (CCPA 1969).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hemant M. Desai whose telephone number is (571) 272-4458. The examiner can normally be reached on 7:00 AM-5: 30 PM, Mon-Thurs..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rinaldi I. Rada can be reached on (571) 272-4467. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hemant M Desai
Examiner
Art Unit 3721

HMD

Stephen F. Gerrity
Primary Examiner
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